| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/649,153 | 08/27/2003 | Masahiko Mizuta | P8388a | 5017 |

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| EXAMINER |
|---|
| WILSON, YOLANDA L |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2113 | |

DATE MAILED: 04/07/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

| | Application No. | Applicant(s) |
|---|---|---|
| **Office Action Summary** | 10/649,153 | MIZUTA ET AL. |
| | Examiner | Art Unit | |
| | Yolanda L. Wilson | 2113 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on <u>*27 August 2003*</u>.

2a)☐ This action is **FINAL**.   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-11* is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☒ All   b)☐ Some * c)☐ None of:

        1.☒ Certified copies of the priority documents have been received.

        2.☐ Certified copies of the priority documents have been received in Application No. _____.

        3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1)☒ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
    Paper No(s)/Mail Date <u>*08/27/03*</u>.

4)☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____ .

5)☐ Notice of Informal Patent Application (PTO-152)

6)☐ Other: _____.

## DETAILED ACTION

### *Specification*

1.      The abstract of the disclosure is objected to because the references to the

locations of the components within the figures need to be removed.  Correction is

required.  See MPEP § 608.01(b).

### *Claim Rejections - 35 USC § 102*

2.      The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that

form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3.      Claims 1-11 rejected under 35 U.S.C. 102(e) as being anticipated by Tabe et al.

(USPN 6622184B1). As per claim 1, Tabe et al. discloses N number of first circuits that

are respectively connected between a predetermined N number (N is a natural number

smaller than M) of the functional blocks among the M number of functional blocks and

the operation processing circuit, and that, in response to an instruction, transfer data,

programs or program instructions between the N number of the functional blocks and

the operation processing circuit in column 3, line 64 – column 4, line 8 and Figure 2;

a second circuit that, when connected to the debug tool, controls the operation

processing circuit in response to an instruction from the debug tool, and instructs the N

number of the first circuits not to transfer data, programs or program instructions

between the N number of the functional blocks and the operation processing circuit in

column 3, lines 55-63; and

a third circuit that, upon receiving predetermined data or a signal, instructs the N

number of the first circuits according to the predetermined data or signal to transfer

data, programs or program instructions between the functional blocks and the operation

processing circuit regardless of an instruction from the second in column 3, lines 38-63.

wherein the operation processing circuit, when not connected to the debug tool,.

transfers and receives data, programs or program instructions to and from the M

number of the functional blocks to execute predetermined operations, and when

connected to the debug tool, reads and transfers to the debug tool data, programs or

program instructions in the N number of the function blocks through the N number of the

first circuits in column 3, line 64 – column 4, line 8. The CPU handles the debugging

when attached to the debug tool and the CPU handles the normal operations of the

processing system, as is known for debugging. The first circuit is the control circuit, the

functional blocks are the rom and the peripheral circuits, the operating processing circuit

is the CPU, the second circuit is the on-chip debug circuit, the third circuit is the security

circuit.

4.      As per claim 2, Tabe et al. discloses wherein the third circuit receives a plurality

of predetermined data or signals, and instructs individual ones of the N number of the

first circuits according to the plurality of predetermined data or signals to transfer data,

programs or program instructions between the functional blocks and the operation

processing circuit, regardless of an instruction from the second circuit in column 3, lines 38-63.

5.      As per claim 3, Tabe et al. discloses wherein the third circuit receives encoded data or signals, decodes the encoded data or signals, and instructs individual ones of the N number of the first circuits according to the decoded data or signals to transfer data, programs or program instructions between the functional blocks and the operation processing circuit, regardless of an instruction from the second circuit in column 3, lines 38-63.

6.      As per claim 4, Tabe et al. discloses wherein the third circuit comprises a register, and when the register is accessed, instructs the N number of the first circuits to transfer data, programs or program instructions between the functional blocks and the operation processing circuit, regardless of an instruction from the second circuit in column 3, lines 38-63.

7.      As per claim 5, Tabe et al. discloses wherein the third circuit, when predetermined data is written in the register, instructs individual ones of the N number of the first circuits according to the data written in the register to transfer data, programs or program instructions between the functional blocks and the operation processing circuit, regardless of an instruction from the second circuit in column 3, lines 38-63. The individual ones are based on the data received to debug select components.

8.      As per claim 6, Tabe et al. discloses wherein the third circuit comprises a plurality of registers, and when the registers are accessed, instructs particular ones of the N number of the first circuits according to the registers accessed to transfer data,

programs or program instructions between the functional blocks and the operation

processing circuit, regardless of an instruction from the second circuit in column 3, lines

38-63. The particular ones are based on the data received to debug select components.

9.      As per claim 7, Tabe et al. discloses wherein the third circuit is comprises a

plurality of registers, and when predetermined data is written in any or all of the

registers, instructs particular ones of the N number of the first circuits according to the

registers accessed and the predetermined data written in the registers to transfer data,

programs or program instructions between the functional blocks and the operation

processing circuit, regardless of an instruction from the second circuit in column 3, lines

38-63. The particular ones are based on the data received to debug select components.

10.     As per claim 8, Tabe et al. discloses wherein the predetermined data or signal

that is received by the third circuit is supplied from the operation processing circuit or

from outside the semiconductor device in column 4, lines 16-21.

11.     As per claim 9, Tabe et al. discloses wherein the register is accessed from the

operation processing circuit or from outside the semiconductor device in column 4, lines

16-21.

12.     As per claim 10, Tabe et al. discloses further comprising a fourth circuit that

receives data in a predetermined protocol from outside the semiconductor device, and

wherein the fourth circuit outputs the predetermined data or signal to the third circuit

based on data received from outside the semiconductor device in column 3, line 64 –

column 4, line 8. The fourth circuit is the control circuit.

13.      As per claim 11, Tabe et al. discloses an in-circuit emulator equipped with a

semiconductor device according to claim 1, and a debug tool that is connected to the

operation processing circuit and the second circuit within the semiconductor device in

Figure 2 and in column 3, line 64 – column 4, line 8.


Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Yolanda L. Wilson whose telephone number is (571)

272-3653. The examiner can normally be reached on M-F (7:30-4:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Robert Beausoliel can be reached on (571) 272-3645. The fax phone

number for the organization where this application or proceeding is assigned is 571-

273-8300.

Information regarding the status of an application may be obtained from the

Patent Application Information Retrieval (PAIR) system. Status information for

published applications may be obtained from either Private PAIR or Public PAIR.

Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

you have questions on access to the Private PAIR system, contact the Electronic

Business Center (EBC) at 866-217-9197 (toll-free).

Yolanda L Wilson
Examiner
Art Unit 2113